AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Please amend the paragraph on page 1, beginning on line 25, as follows:

Voltage Vb is applied to an electrode of the capacitive sensor Cs and other electrode is connected to an input terminal of the buffer amplifier 12 via the signal wire 13. The input protection circuit 11 is a circuit that clamps high voltage, such as the voltage caused by static electricity ~~diving into~~ accumulated in the signal wire 13 ~~to supply voltage~~, and is composed of diodes Dp and Dm connected between the signal wire 13 and positive power supply (+Vdd) and negative power supply (–Vdd).

Please amend the paragraph on page 2, beginning on line 1, as follows:

The conventional capacitance detection circuit 10 ~~like this acts~~ operates as follows.

Please amend the paragraph on page 2, beginning on line 24, as follows:

Here, when Vb is ~~direct~~ DC voltage, only AC component Vo of the output voltage Vout corresponding to a variance in physical quantity is a final signal. Therefore, the AC component Vo is:

$Vo = Vb \cdot \Delta C / (Cd + \Delta C + Ci)$ -- (Equation 1)

Please amend the paragraph on page 3, beginning on line 5, as follows:

FIG. 2 is an equivalent circuit diagram when the capacitance detection circuit 10 shown in FIG. 1 operates normally (when diodes Dp and Dm are reversely biased.) Here, capacitance of diode Dp and capacitance of diode Dm (depletion layer capacitance when being reversely biased) are illustrated as capacitors Cdp and Cdm, respectively and input capacitance of the buffer amplifier 12 is illustrated as a capacitor Cg. The parasitic capacitance Ci is a total value of capacitance of these capacitors, Cdp, Cdm and Cg:

Ci = Cdp + Cdm + Cg

All of them, however, are parasitic capacitance produced by an essential circuit including the diode Dp, the diode Dm, and the buffer amplifier 12.

Please amend the paragraph on page 3, beginning on line 16, as follows:

Here, if it is possible to form the whole capacitance detection circuit 10 with a ~~one-tip IC~~ one-chip IC, it is possible to reduce the parasitic capacitance Ci substantially without providing the input protection circuit 11. However, when it is necessary to produce a product by assembling two or more kinds of parts or to implement a capacitive sensor Cs and a detection circuit at positions far apart or the like, it is inevitable to implement a capacitance detection circuit with a structure in which the capacitive sensor Cs and the detection circuit are separated. It is, therefore, unavoidable to provide the input protection circuit 11 in the input stage of the buffer amplifier 12. Consequently, parasitic capacitance caused by the input protection circuit

11 is added and there is a problem that the sensitivity of the capacitance detection circuit deteriorates.